

FEATURES

- Ultralow rms jitter: 50 fs (12 kHz to 20 MHz, typical)
- Noise floor: -156 dBc/Hz at 2456.76 MHz
- Low phase noise: <-142 dBc/Hz at 800 kHz, 983.04 MHz output
- Up to 14 LVDS, LVPECL, or CML type device clocks (DCLKs) from PLL2
- Maximum CLKOUTx/SCLKOUTx frequency up to 3200 MHz
- JESD204B-compatible system reference (SYSREF) pulses 25 ps analog, and $\frac{1}{2}$ VCO cycle digital delay independently programmable on each of 14 clock output channels
- SPI-programmable phase noise vs. power consumption
- Narrow-band, dual core VCOs
- Up to 2 buffered voltage controlled oscillator (VCXO) outputs
- Up to 4 input clocks in LVDS, LVPECL, CMOS, and CML modes
- Supports deterministic synchronization of multiple HMC7044 devices with pin or SPI controlled SYNC trigger
- Frequency holdover mode to maintain output frequency
- Loss of signal (LOS) detection and hitless reference switching
- 4x GPIOs alarms/status indicators to determine the health of the system
- External VCO input to support up to 5 GHz
- On-board regulators for excellent PSRR
- 68-lead, 10 mm x 10 mm LFCSP package

APPLICATIONS

- JESD204B clock generation
- Cellular infrastructure (multicarrier GSM, LTE, W-CDMA)
- Data converter clocking
- Microwave baseband cards
- Phase array reference distribution

GENERAL DESCRIPTION

The HMC7044 is a high performance dual-loop integer N jitter attenuator capable of performing reference selection and generation of ultralow phase noise frequencies for high speed data converters with either parallel or serial (JESD204B type) interfaces. The HMC7044 features two integer mode PLLs and overlapping on-chip VCOs that are SPI-selectable with wide tuning ranges around 2.5 GHz and 3 GHz, respectively. The device is designed to meet the requirements of GSM and LTE base station designs, and offer a wide range of clock management and distribution features to simplify baseband and radio card clock tree designs. The HMC7044 provides 14 low noise and configurable outputs to offer flexibility in interfacing with many different components including data converters, field-programmable gate arrays (FPGAs), and mixer local oscillators (LOs).

The DCLK and SYSREF clock outputs of the HMC7044 can be configured to support signaling standards, such as CML, LVDS, LVPECL, and LVCMOS, and different bias settings to offset varying board insertion losses.

FUNCTIONAL BLOCK DIAGRAM

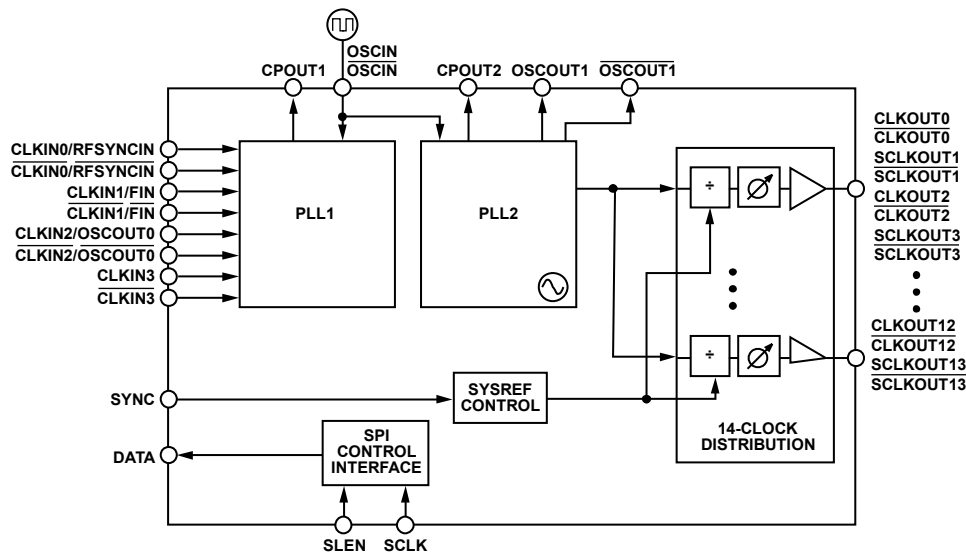


Figure 1.

For more information about the HMC7044, contact Analog Devices, Inc., at RFMG-timing@analog.com.

Rev. PrA

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